CLAIMS

What is claimed is:

1. A processor comprising:

a first memory to store instructions and data for use by the processor, the first memory further to store data representing a first state of a cellular automaton at a first time step, the data to be organized in cells;

a first update engine; and

a cellular automaton update unit to provide data from selected cells of the cellular automaton to the first update engine,

the first update engine to update at least some of the selected cells according to an update rule and a state of any associated neighborhood cells to provide a state of the cellular automaton at a second time step.

2. The processor of claim 1 further comprising:

a cellular automaton prefetch state machine to prefetch data from cells to be updated and associated neighborhood cells.

3. The processor of claim 2 wherein

the cellular automaton prefetch state machine is further to write data representing the second state of the cellular automaton back to the first memory.

4. The processor of claim 2 further comprising:

data rasterizer control circuitry, the data rasterizer control circuitry, together with the cellular automaton prefetch state machine to rasterize prefetched data.

5. The processor of claim 4 further comprising:

a neighborhood buffer, the neighborhood buffer to store prefetched, rasterized data for use by the update engine.

6. The processor of claim 5 wherein the first memory comprises a first cache memory and the neighborhood buffer comprises a second cache memory.

7. The processor of claim 5 wherein the neighborhood buffer comprises a cache line buffer.

8. The processor of claim 5 further comprising:

shifter logic to select from the neighborhood buffer a cell to be updated and associated neighborhood cells, the shifter logic further to present data associated with the selected cells to the update engine.

9. The processor of claim 1 further comprising:

a second update engine, wherein the first and second update engines are pipelined, the first update engine to update the cellular automaton to provide the second state of the cellular automaton at the second time step, the second

update engine to update the second state of the cellular automaton to provide a third state of the cellular automaton at a third time step.

10. The processor of claim 9 further comprising:

a cellular automaton prefetch state machine, the cellular automaton prefetch state machine to write data representing the third state of the cellular automaton back to the first memory.

11. A microprocessor comprising:

a cache memory hierarchy including at least two levels of cache memory, a first level of the cache memory to store data representing a first state of a cellular automaton at a first time step, the data being organized in cells;

an execution cluster including at least a first execution unit to execute microprocessor instructions; and

a cellular automaton update unit, the cellular automaton update unit to provide data associated with cells of the cellular automaton to the first execution unit, the first execution unit to update each cell to be updated in the cellular automaton in response to an update rule and in response to a state of any associated neighborhood cells at the first time step to provide a second state of the cellular automaton at a second time step.

12. The microprocessor of claim 11 wherein

the execution cluster further comprises at least a second execution unit, the first and second execution units being pipelined to update the cellular automaton at least twice before associated data is written back to the first level of the cache memory hierarchy.

13. The microprocessor of claim 12 wherein the cellular automaton update unit comprises:

data rasterizer control circuitry, the data rasterizer control circuitry in conjunction with a prefetch state machine to rasterize data associated with the cellular automaton cells to be provided to the first execution unit, and

one or more shifters, the one or more shifters to shift the rasterized data past the first execution unit and to shift data associated with the second state of the cellular automaton past the second execution unit.

14. The microprocessor of claim 13 wherein the cellular automaton update unit further comprises:

a data store to store data associated with a cell at the second time step and all associated neighborhood cells until all the associated neighborhood cells have been updated by the first execution engine.

15. The microprocessor of claim 11 further comprising:

a prefetch state machine, the prefetch state machine to prefetch data associated with the cell to be updated and associated neighborhood cells.

16. The microprocessor of claim 15 wherein the cellular automaton update unit comprises:

data rasterizer control circuitry, the data rasterizer control circuitry in conjunction with the prefetch state machine to rasterize prefetched data to be provided to the first execution unit.

17. The microprocessor of claim 16 wherein the cellular automaton update unit further comprises:

one or more shifters to shift the rasterized data past the first execution unit.

18. The microprocessor of claim 11 further including a microcode read-only memory, the microcode read only memory to include microcode to support at least one cellular automaton-specific operation.

19. A method comprising:

storing data representing a state of a cellular automaton at a first time step in a memory of a general-purpose processor;

rasterizing a portion of the stored data, the portion including at least data associated with a cell to be updated and associated neighborhood cells;

updating the cell to be updated according to an update rule and a state of the associated neighborhood cells at the first time step; and

repeating rasterizing and updating until all cells to be updated have been updated such that a state of a cellular automaton at a second time step is provided.

20. The method of claim 19 further comprising:

writing back to the memory data representing the updated state of the cellular automaton.

21. The method of claim 20 further comprising:

updating the cellular automaton for multiple time steps prior to writing back to the memory.

22. A system comprising:

a bus to communicate information;

a device coupled to the bus to enable access to a medium storing an application including a cellular automaton; and

a general-purpose processor coupled to the bus to execute the application, the general-purpose processor including:

a memory to store data representing a state of the cellular automaton at a first time step, the data being organized in cells,

an execution cluster including a first execution unit; and

a cellular automaton update unit to provide data associated with cells of the cellular automaton to the first execution unit, the first execution

unit to update each cell to be updated in the cellular automaton in response to an update rule and in response to a state of any associated neighborhood cells at the first time step to provide a second state of the cellular automaton at a second time step.

23. The system of claim 22 wherein the device is a mass storage unit.

24. The system of claim 22 wherein the device is a network connection device.

25. The system of claim 22 wherein the processor further includes a cellular automaton prefetch state machine to prefetch data to be provided to the execution unit.

26. The system of claim 25 wherein the cellular automaton prefetch state machine is further to write data representing the state of the cellular automaton at the second time step back to the memory.

27. The system of claim 22 wherein the memory is an on-processor cache memory.

28. The system of claim 23 wherein the processor further includes

a cellular automaton prefetch state machine to control prefetching of data to be provded to the execution unit and wherein,

the memory is a first on-chip cache memory, the processor further including a second on-chip cache memory to store the prefetched data.

29. The system of claim 22 wherein the processor further includes

a second execution unit pipelined with the first execution unit to update the cellular automaton multiple times before an updated state is written back to the memory.